

DUBHE-90 CPU IP

A commercial 64-bit RISC-V CPU IP that supports a rich set of RISC-V extensions, enabling edge, cloud computing, and high-performance applications.

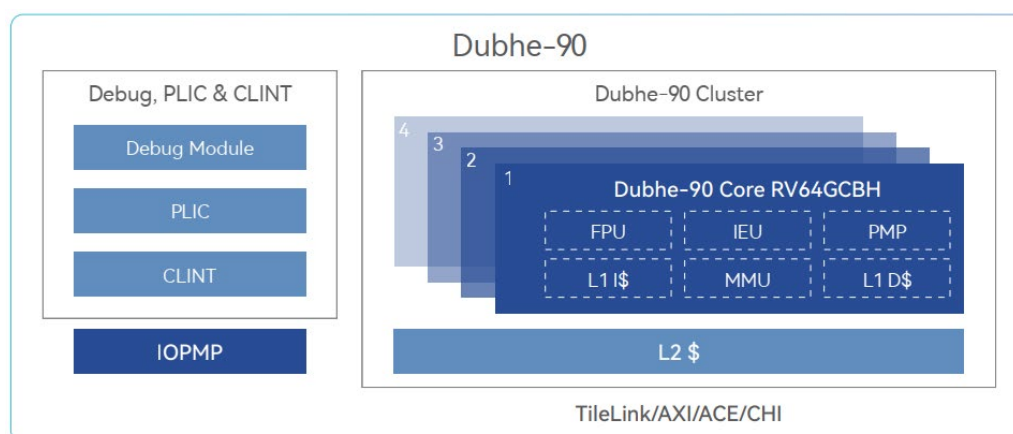
INTRODUCTION

StarFive Dubhe-90 processor features an 11+ stage and 5-issue pipeline, superscalar, and deep out-of-order execution, and supports standard RISC-V RV64GCBH extensions. With a score of 9.4 SPECint2006/GHz, Dubhe-90 is designed for high-performance computing scenarios and devices, such as data centers, PCs, mobile devices, high-performance network communications, and machine learning.

Dubhe-90 has been pre-integrated and verified, making it easy to use for SoC development work. With options of single-core, dual-core, or quad-core in a single cluster with memory coherency, Dubhe-90 is highly scalable.

ISA

| | |
|-------------|-------|
| RV64I | 2.1 |
| M | 2.0 |
| A | 2.1 |
| F | 2.2 |
| D | 2.2 |
| C | 2.0 |
| B | 1.0 |
| Priv. Spec. | 1.12 |
| H | 0.6.1 |
| Debug | 0.13 |
| Trace | 1.0 |



DESIGN SPECIFICATIONS

- SPECint2006: 9.4/GHz
- Dhrystone: 6.5/Mhz (Legal)
- Support Hypervisor (H) extension
- 11+ stage, 5-issue pipeline
- Superscalar, deep out-of-order execution
- Support for multi-core cache coherence

EDGE / CLOUD DATA CENTERS

- Edge Cloud Computing
- SmartNIC and DPU
- Enterprise-level computational storage
- BMC

COMMUNICATION / NETWORKING

- 5G Architecture and base station
- Wireless Access Point
- Enterprise Switch and Firewall / NGFW
- V2X Communication

AI / ML

- AV/ADAS
- IVI/Cluster/HUD
- Robots/Drones/Industrial Control
- Computer Vision/AR/VR/MR

FUNCTION LIST

IFU

- Decoupled structure of instruction fetch and branch prediction
Fetch width: 16 byte per cycle
- Fetch width: 16 byte per cycle
- RAS predictor for return instruction
- IJTP predictor for indirect-jump instruction
- TAGE style predictor for conditional branch instruction

TKU

- 5-Way Decode/Rename/Commit
- ROB Entries: 160
- Integer physical register file entries: 160
- Floating-point physical register file entries: 160

IEU

- 2 independent full ALU units
- 1 full ALU unit reusing MDU resources
- 1 independent branch execution unit

FPU

Support the IEEE 754-2008 floating-point standard for 32-bit single-precision and 64-bit double-precision arithmetic

MMU

- Support bare, Sv39, and Sv48 modes, as defined in the RISC-V Priv. Spec
- Support 32-entry fully-associative ITLB
- Support 48-entry DTLB
- Support 1280-entry 5-way set associative STLB

MEMORY SUB-SYSTEM

- L1 instruction cache
 - Configurable set-associative instruction cache
 - Default 64 KB, 4-way set associate
 - Support data prefetch
 - Optional parity check
- L1 data cache
 - Default 64 KB, 4-way set associate
 - Two load/store pipes
 - Support cache writing policy: write-back
 - Out-of-order processing, non-blocking cache design
 - Support custom CMO instructions
 - Optional ECC
- L2 cache
 - Default 2 MB, 8-way set associate
 - Support L2 cache prefetch
 - MESI coherency
 - Support cache writing policy: write-back
 - Core cluster level shared between cores
 - Optional ECC

PMP & PMA

- Support 16 regions with a minimum region size of 4096 bytes
- Support fixed PMA

FUNCTION LIST

IOPMP

- Check access request permissions initiated by different master devices
- Record the source of invalid memory access requests initiated by master devices
- Support up to 64 master device sources (SRCID)
- Support address and permission configuration for 16 memory access domains

HPM

- RISC-V standard hardware performance monitor support
- Help micro-architecture level analysis and performance tuning

POWER MANAGEMENT

- Core level Wait For Interrupt mechanism
- Core and cluster level clock gating
- Core and cluster level low-power states (Power ON/OFF/Retention)
- Cluster-level frequency scaling

DEBUG

Standard RISC-V trace interface support

PLIC

- PLIC Interrupts: 1,024 configurable interrupt signals, which can be connected to devices outside the core subsystem.
- PLIC priority levels: PLIC supports 8 priority levels

CLINT

Up to 32 configurable interrupt targets or harts

TRACE

Standard RISC-V trace interface support

SOFTWARE DEVELOPMENT

- Bare Metal SDK
 - Compiler and toolchains, including two packages based on GCC and LLVM frameworks
 - GDB debugger and pre-built OpenOCD
 - FreeRTOS
 - Sample projects
- Linux SDK
 - Yocto-based environment
 - Kernel 6.1
 - Host development tools
 - QSPI image on target
 - OpenSBI
 - KVM
 - Xvisor
 - Eclipse IDE
- 27 sample projects
- StarFive StarStudio
 - Provide stand-alone and pre-built IDE for customers