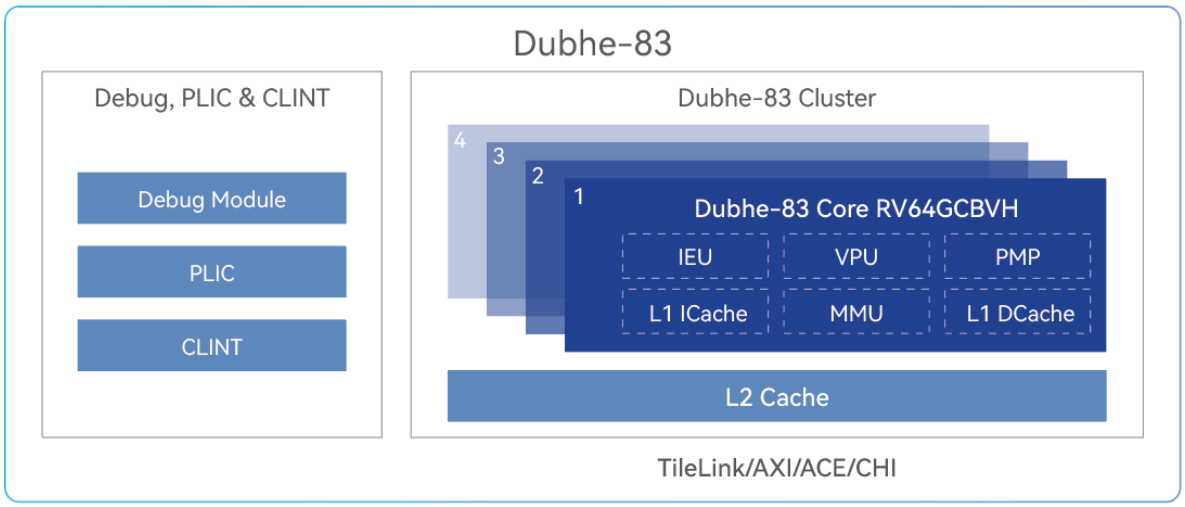
DUBHE-83 CPU IP

Dubhe-83 CPU IP is a commercial-grade 64-bit RISC-V CPU IP that supports Vector, enabling high-efficiency applications.

INTRODUCTION

StarFive Dubhe-83 CPU IP features a 10+ stage pipeline, 3-issue, and out-of-order pipeline, follows the RVA23 Profile, and supports all extensions of Vector Crypto. With a score of 8.5 SPECInt2006/GHz, Dubhe-83 targets applications that require highly energy-efficient computation, including mobile, desktop, AI, and automotive.

Dubhe-83 has been pre-integrated and verified, making it easy to use for SoC development work. With options of single-core, dual-core, or quad-core in a single cluster with memory coherency, Dubhe-83 is highly scalable.



DESIGN SPECIFICATIONS

- SPECint2006: 8.5/GHz
- Dhrystone: 6.0/Mhz (Legal)
- ISA：RV64GCBVH
- 10-stage+ pipeline, 3-issue
- Superscalar, deep out-of-order execution
- Support for multi-core cache coherence

MOBILE APPLICATION	INDUSTRIAL CONTROL	AI
• Smart Phone	• HMI	• Robots
• Tablet	• Industrial Display	• Computer Vision
• Smart Wear	• Industrial Inspection	• Smart Home
• Game Devices	• Smart home gateway	

FUNCTION LIST

IFU

- An architecture that decouples instruction fetching from branch prediction
- fetch width: 16 byte per cycle
- RAS predictor for return instruction
- IJTP predictor for indirect-jump instruction
- TAGE style predictor for conditional branch instruction

TKU

- 3-Way Decode/Rename/Commit
- ROB Entries: 128
- Integer Physical Register File Entries: 128
- Floating-point/Vector physical register file entries: 192

IEU

- 3 Full ALU (Arithmetic/Logic) units
- 1 MDU (Multiply/Divide) unit
- 1 BRU (Branch/Jump) unit

VPU

- Supports 8-bit, 16-bit, 32-bit, and 64-bit integer operations, as well as IEEE 754-2008 standard 16-bit, 32-bit, 64-bit floating-point operations and BF16 floating-point operations.
- Supports VLEN=DLEN=256
- 2 vector pipeline units
- 2 floating-point pipeline units

MMU

- Support Bare, Sv39, and Sv48 modes, as defined in the RISC-V Priv. Spec
- Support 32-entry fully-associative L1 ITLB
- Support 32-entry fully-associative L1 DTLB
- Support 1024-Entry set associative STLB
- Optional parity checking

Memory Sub-system

- L1 instruction cache
  - Configurable set-associative instruction cache
  - Default 32 KB, 4-way associate
  - Support way-prediction
  - Optional parity checking
- L1 data cache
  - Default 32 KB, 4-way set-associate
  - Two load/store pipes
  - Support cache writing policy: write-back
  - Out-of-order processing, non-blocking cache design
  - Support way-prediction
  - Support standard CMO 1.0
  - Optional ECC
- L2 cache
  - Default 512 KB, 8-way set associate
  - MESI Coherency
  - Hardware data prefetching
  - Support cache writing policy: write-back
  - Core cluster level shared between cores
  - Optional ECC

FUNCTION LIST

PMP&PMA

- Support 16/32/64 regions with a minimum region size of 4096 bytes
- Support predefined PMA and Svpbmt

HPM

- RISC-V standard Hardware performance monitor support
- Help micro-architecture level analysis and performance tuning

Power Management

- Core level Wait For Interrupt mechanism
- Core land cluster level clock gating
- Core and cluster level low-power states (Power ON/OFF/Retention)
- Cluster-level frequency scaling

PLIC

- PLIC Interrupts: 1,024 configurable interrupt signals, which can be connected to devices outside the core subsystem.
- PLIC Priority Levels: PLIC supports 8 priority levels

CLINT

- Up to 32 Configurable interrupt targets or harts

Debug

- Standard RISC-V debug support

Trace

- Standard RISC-V trace interface support

Software Development

- Bare Metal SDK
  - Compiler and toolchains, including two packages based on GCC and LLVM frameworks
  - GDB debugger and pre-built OpenOCD
  - FreeRTOS
  - 36+ sample projects
- Linux SDK
  - Yocto-based environment
  - Kernel 6.6
  - Host development tools
  - OpenSBI
  - Uboot
  - KVM
  - Xvisor
- StarFive StarStudio
  - Provide stand-alone and pre-built IDE for customers