DUBHE-80 CPU IP

A 64-bit commercial RISC-V CPU IP with rich RISC-V extensions support, targeting highly energy-efficiency applications.

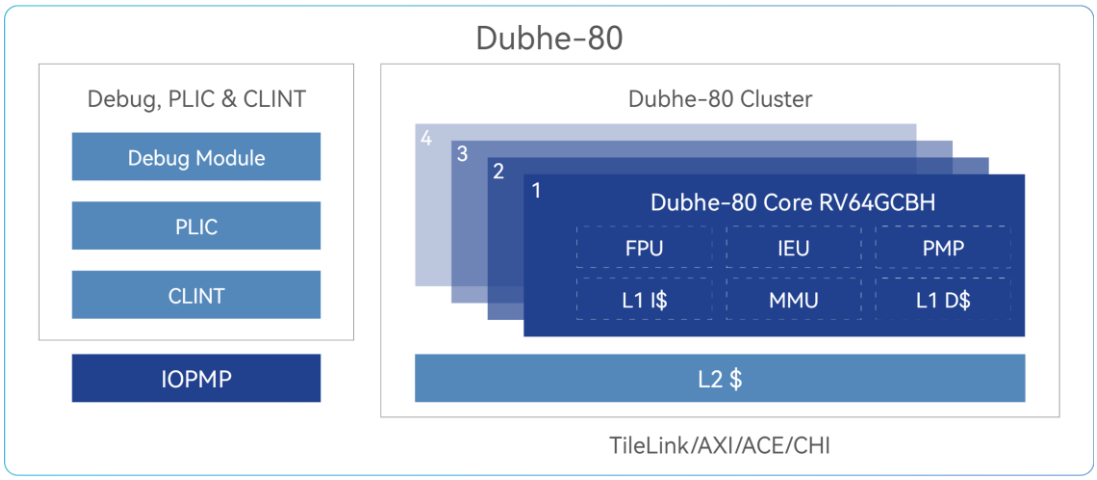
OVERVIEW

StarFive Dubhe-80 processor features a 9+ stage, 3-issue, out-of-order pipeline, fully compliant with RV64GCBH specifications. With a score of 8.0 SPECInt2006/GHz, Dubhe-80 is designed for mobile, desktop, AI, and automotive applications that require highly energy-efficient computation.

Dubhe-80 has been pre-integrated and verified, making it easy to use for SoC development work. With options of single-core, dual-core, or quad-core in a single cluster with memory coherency, Dubhe-80 is highly scalable.

ISA

RV64I	2.1
M	2.0
A	2.1
F	2.2
D	2.2
C	2.0
B	1.0
Priv. Spec.	1.12
H	0.6.1
Debug	0.13
Trace	1.0



DESIGN SPECIFICATIONS

- SPECint2006: 8.0/GHz
- Dhrystone: 6.0/Mhz (Legal)
- ISA: RV64GCBH
- 9+ stage, 3-issue pipeline
- Superscalar, deep out-of-order execution
- Support for multi-core cache coherence

MOBILE

- Smart Phone
- Tablets
- Smart Wear
- Game Devices

AUTOMOTIVE

- Car entertainment
- Intelligent Cockpit
- V2V Communication
- Automated Driving

AI

- Robotics
- Computer Vision
- Smart Home

FUNCTION LIST

IFU

- Decoupled structure of instruction fetch and branch prediction
- Fetch width: 16 byte per cycle
- RAS predictor for return instruction
- IJTP predictor for indirect-jump instruction
- TAGE style predictor for conditional branch instruction

TKU

- 3-Way Decode/Rename/Commit
- ROB entries: 128
- Integer physical register file entries: 128
- Floating-point physical register file entries: 96

IEU

- 2 independent full ALU
- 1 full ALU reusing MDU resources
- 1 independent branch execution unit

FPU

- Support the IEEE 754-2008 floating-point standard for 16-bit half-precision, 32-bit single-precision and 64-bit double-precision arithmetic
- Support BF16
- Dual symmetric pipeline

MMU

- Support bare, Sv39, and Sv48 modes, as defined in the RISC-V Priv. Spec
- Support 32-entry fully-associative L1 ITLB
- Support 32-entry fully-associative L1 DTLB
- Support 1024-entry set associative STLB
- Optional parity check

Memory Sub-system

- L1 instruction cache
  - Configurable set-associative instruction cache
  - Default 32 KB, 4-way associate
  - Optional parity check
- L1 data cache
  - Default 32 KB, 4-way associate
  - Two load/store pipes
  - Support cache writing policy: write-back
  - Out-of-order processing, non-blocking cache design
  - Support custom CMO instructions
  - Optional ECC
- L2 cache
  - Default 512 KB, 8-way set associate
  - MESI coherency
  - Support cache writing policy: write-back
  - Core cluster level shared between cores
  - Optional ECC

FUNCTION LIST

PMP&PMA

- Support 16 regions with a minimum region size of 4096 bytes
- Support fixed PMA

HPM

- RISC-V standard hardware performance monitor support
- Help micro-architecture level analysis and performance tuning

Power Management

- Core level Wait For Interrupt mechanism
- Core land cluster level clock gating
- Core and cluster level low-power states (Power ON/OFF/Retention)
- Cluster-level frequency scaling

PLIC

- PLIC Interrupts: 1,024 configurable interrupt signals, which can be connected to devices outside the core subsystem.
- PLIC Priority Levels: PLIC supports 8 priority levels

CLINT

- Up to 32 configurable interrupt targets or harts

Debug

- Standard RISC-V debug support

Trace

- Standard RISC-V trace interface support

IOPMP

- Check access request permissions initiated by different master devices
- Record the source of invalid memory access requests initiated by master devices
- Support up to 64 master device sources (SRCID)
- Support address and permission configuration for 16 memory access domains

Software Development

- Bare Metal SDK
  - Compiler and toolchains, including two packages based on GCC and LLVM frameworks
  - GDB debugger and pre-built OpenOCD
  - FreeRTOS
  - Sample projects
- Linux SDK
  - Yocto-based environment
  - Kernel 6.1
  - Host development tools
  - QSPI image on target
  - OpenSBI
  - KVM
  - Xvisor
  - Eclipse IDE
- 29 sample projects
- StarFive StarStudio
  - Provide stand-alone and pre-built IDE for customers