DUBHE-70 CPU IP

Dubhe-70 is an ultra-low power consumption out-of-order commercial-grade 64-bit RISC-V CPU IP.

INTRODUCTION

StarFive Dubhe-70 is a 9+ stage, 3-issue, out-of-order CPU IP that supports the rich RISC-V instruction set, RV64GCBH_Zicond_Zicbom_Zicboz_Zicbop.

With a score of 7.2 SPECInt2006/GHz, Dubhe-70 targets applications that require highly energy-efficient computation, including mobile, desktop, AI, and automotive.

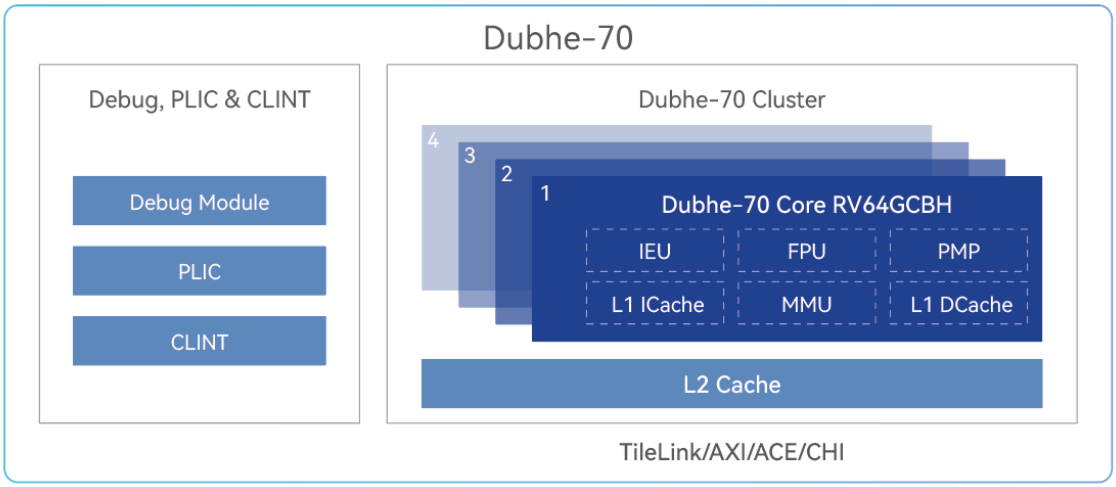
Dubhe-70 has been pre-integrated and verified, making it easy to use for SoC development work.

With options of single-core, dual-core, or quad-core in a single cluster with memory coherency, Dubhe-70 is highly scalable.

Dubhe-70's energy efficiency is 21% higher compared to Dubhe-80.

EXTENSIONS

RV64I	2.1	Debug	0.13
M	2.0	Trace	1.0
A	2.1	Zicond	1.0
F	2.2	Zicbom	1.0
D	2.2	Zicboz	1.0
C	2.0	Zicbop	1.0
B	1.0	Svnapot	1.0
Priv.	1.12	Svpbmt	1.0
H	1.0	Svinval	1.0



DESIGN SPECIFICATIONS

- SPECint2006: 7.2/GHz
- Dhrystone: 6.0/Mhz (Legal)
- ISA: RV64GCBH
- 9-stage+ pipeline, 3-issue
- Superscalar, deep out-of-order execution
- Support for multi-core cache coherence

MOBILE

- Smart Phone
- Tablet
- Smart Wear
- Game Devices

INDUSTRIAL CONTROL

- HMI
- Industrial Display
- Industrial Inspection
- Smart home gateway

AI

- Robots
- Computer Vision
- Smart Home

FUNCTION LIST

IFU

- An architecture that decouples instruction fetching from branch prediction
- Fetch width: 16 byte per cycle
- RAS predictor for return instruction
- IJTP predictor for indirect-jump instruction
- TAGE style predictor for conditional branch instruction

TKU

- 3-Way Decode/Rename/Commit
- ROB Entries: 80
- Integer Physical Register File Entries: 88
- Floating-Point Physical Register File Entries: 72

IEU

- 3 Full ALU (Arithmetic/Logic) units
- 1 MDU (Multiply/Divide) unit
- 1 BRU (Branch/Jump) unit

FPU

- Support the IEEE 754-2008 floating-point standard for 32-bit single-precision and 64-bit double-precision arithmetic
- 1 floating-point pipeline units

MMU

- Support Bare, Sv39, and Sv48 modes, as defined in the RISC-V Priv. Spec
- Support 16-entry fully-associative L1 ITLB
- Support 24-entry fully-associative L1 DTLB
- Support 1024-Entry set associative STLB
- Optional parity checking

Memory Sub-system

- L1 instruction cache
  - Configurable set-associative instruction cache
  - Default 32 KB, 4-way associate
  - Optional parity checking
- L1 data cache
  - Default 32 KB, 4-way associate
  - Two load/store pipes
  - Support cache writing policy: write-back
  - Out-of-order processing, non-blocking cache design
  - Support custom CMO instructions
  - Optional ECC
- L2 cache
  - Default 128 KB, 8-way set associate
  - MESI Coherency
  - Hardware data prefetching
  - Support cache writing policy: write-back
  - Core cluster level shared between cores
  - Optional ECC

FUNCTION LIST

PMP&PMA

- Support 16/32/64 regions with a minimum region size of 4096 bytes
- Support predefined PMA and Svpbmt

HPM

- RISC-V standard Hardware performance monitor support
- Help micro-architecture level analysis and performance tuning

Power Management

- Core level Wait For Interrupt mechanism
- Core land cluster level clock gating
- Core and cluster level low-power states (Power ON/OFF/Retention)
- Cluster-level frequency scaling

PLIC

- PLIC Interrupts: 1,024 configurable interrupt signals, which can be connected to devices outside the core subsystem.
- PLIC Priority Levels: PLIC supports 8 priority levels

CLINT

- Up to 32 Configurable interrupt targets or harts

Debug

- Standard RISC-V debug support

Trace

- Standard RISC-V trace interface support

Software Development

- Bare Metal SDK
  - Compiler and toolchains, including two packages based on GCC and LLVM frameworks
  - GDB debugger and pre-built OpenOCD
  - FreeRTOS
  - 36 sample projects
- Linux SDK
  - Yocto-based environment
  - Kernel 6.6
  - Host development tools
  - OpenSBI
  - KVM
  - Xvisor
- StarFive StarStudio
  - Provide stand-alone and pre-built IDE for customers