

STARLINK-700 INTERCONNECT FABRIC IP

StarLink-700 is StarFive's self-developed interconnect fabric IP with cache coherence support for a manycore SoC solution.

INTRODUCTION

StarLink-700 is StarFive's self-developed high-scalable, high-performance interconnect fabric IP supporting cache coherence, enabling the construction of a manycore SoC solution.

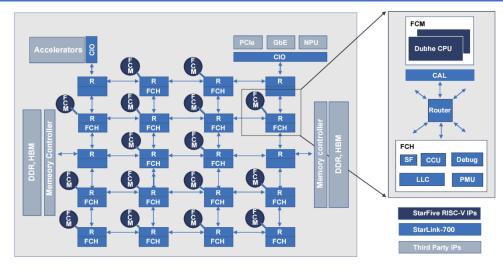
- Providing NoC with cache coherence: connecting up to 256 CPU cores, IO devices, and DDR, while maintaining cache coherence within the SoC scope
- High performance: providing a maximum of 512 MB Last Level Cache (LLC) with Snoop Filter, enhancing the efficiency of coherence maintenance modules and memory hierarchy performance.
- High scalability: employing mesh NoC to enhance expandability, and a dedicated control NoC to support control command transmission
- Low latency: adopting a semi-custom design approach to reduce NoC transmission latency.
- Efficient data exchange: supporting CPU and IO devices to share the LLC, simplifying CPU and IO data exchange, and improving performance
- Low power consumption: supporting low power consumption technologies such as LLC way shutdown and Architecture Clock Gating
- High reliability: Snoop Filter and LLC support ECC (SEC-DED, Single Error Correction Double Error Detection)

DESIGN SPECIFICATIONS

- High bandwidth, low power consumption, low latency
- Support Component Aggregation Layer (CAL)
- Topology: Mesh
- Frequency: 1.5 GHz @ 12nm (Reference)
- Support up to 256 CPU Cores

- Support up to 128 Fully Coherent Master Nodes (FCM)
- Support multiple I/O Coherent Master Nodes (CIO)
- Maximum node count: 12x12
- Single node supports 2-5 devices
- Max memory device ports: 40
 - Configurable data path link width: 128/256/512b

16-CORE SOC SYSTEM SUPPORTED BY STARLINK-700



• FCH: Fully Coherent Home Node : Home node for a coherent region of memory with a block of SLC and Snoop Filter

- FCM: Fully Coherent Master Node: Typically a CPU core, a CAL with two cores, or a CPU core cluster
- CIO: I/O Coherent Master Node: An I/O-coherent master device

FUNCTION LIST

Coherence Unit

- Support manycore CPU core/cluster coherency
- Support CHI protocol
- Support Snoop Filter
- Support cache coherent IO

LLC

- Distributed LLC
- Cache Inclusion Policy: Noninclusive
- Support CMO
- Support atomic

Low Power Design

- Support low power consumption
 mode
 - Architecture Clock Gating
 - Cache Way Shutdown

RAS

 Snoop Filter and LLC supports SEC-DED

CIO Port

Support concurrency

Error Reporting

Support error reporting

Debug

Support debug

Performance Monitor (PMU)

- Support performance monitor
- Support an independent Control NoC for transmitting control commands: PMU, CMO, Interrupt, etc.
- Support Message Signaled Interrupts (MSI)

CONTACT US

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